SEMICONDUCTOR PACKAGING DEVICE AND MANUFACTURE THEREOF

ABSTRACT OF THE INVENTION

A semiconductor packaging device comprises a carrier having at least a cavity or a slot thereon. At least a chip has a back surface and an active surface with a plurality of first bonding pads. The chip is affixed to the cavity to expose the active surface. A first insulating layer is on the active surface and the carrier, which comprises first plating through holes connected to first bonding pads and via the first insulating layer. A multi-layer structure is on the first insulating layer, which comprises conductive layout lines, second plating through holes therein, and a second insulating layer and exposed ball pads thereon. The first plating through holes are electrically connected with the conductive layout lines, the second plating through holes, and the exposed ball pads. A plurality of solder balls are affixed to the ball pads. Such architecture integrates the redistribution and fan-out process, which simplifies the conventional process for flip-chip ball grid array.